B: Amendments to The Claims:
Amend the claims to read as follows:

Claim 1. (Currently Amended) A multiprocessor computer system comprising,

a cache coherent symmetric (SMP) computer system of symmetric multiple processors having a plurality of processing nodes and caches and a node controller which use processor state information according to mappings provided by supervisor software or firmware of allowable physical processors to an application workload to determine which coherent cache regions in the system are required to examine a coherency transaction produced by a storage request of a single originating processor of said computer system and to change coherency boundaries of one or more of said coherent cache regions directly with coherency mode bits for said coherent cache regions, and wherein a control program for the dispatch of virtual processors for controlling the size and extent of a required coherency domain changes said coherency boundaries directly with said coherency mode bits.

Claim 2. (Previously Amended) The multiprocessor computer system according to claim 1 wherein a node of said plurality of processing nodes of the computer has dynamic coherency boundaries such that hardware of said computer system uses only a subset of the processors in said computer system for a single workload at any specific point in time and optimizes the cache coherency as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload.

Claim 3. (Previously Amended) The multiprocessor computer system according to claim 1 wherein multiple instances of a physical node are connected with a second level controller

to create a multiprocessor system having multiple node controllers.

Claim 4. (Original) The multiprocessor computer system according to claim 1 wherein said node controller uses mode bits to determine which processors must receive any given transaction that is received by the node controller.

Claim 5. (Previously Amended) The multiprocessor computer system according to claim 1 wherein a second level controller is provided which uses mode bits to determine which nodes must receive any given transaction that is received by the second level controller.

Claim 6. (Previously Amended) The multiprocessor computer system according to claim 1 wherein logical partitions are provided and mapping of said logical partitions to allowable physical processors is provided by supervisor software or firmware of allowable physical processors to an application workload.

Claim 7. (Previously Amended) The multiprocessor computer system according to claim 1 wherein logical partitions are provided for the supervisor software or firmware which maps allowable physical processors to an application workload and a hypervisor assigns cache coherence regions which encompass subsets of said processors and caches in the system chosen for their physical proximity and defines a distinct cache coherency region for each of said logical partitions.

Claim 8. (Previously Amended) The multiprocessor computer system according to claim 1 wherein a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time for an assigned partition and a distinct cache coherency for the

address space of the assigned partition as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload in said assigned partition.

Claim 9. (Previously Amended) The multiprocessor computer system according to claim 1 wherein a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time, and multiple cache coherent regions are assigned for different partitions as more independent workloads coexist on said hardware.

Claim 10. (Previously Amended) The multiprocessor computer system according to claim 1 wherein cache coherence regions encompass subsets of processors and caches in the computer system and a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time for an assigned partition and a distinct cache coherency for the address space of the assigned partition as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload in said assigned partition.

Claim 11. (Previously Amended) The multiprocessor computer system according to claim 1 wherein software and/or firmware define which subset of processors in said multiprocessor must participate in a coherency transaction independent of which processing node is connected to physical DRAM storage being requested by said single originating processor.

Claim 12. (Previously Amended) The multiprocessor computer system according to claim 11 wherein the movement of a process between nodes of said symmetric multiple processors

of said multiprocessor is effectuated without moving physical storage contents and without requiring subsequent broadcasting of the storage references originated by the process from said single originating processor's storage request to all of the caches in the multiprocessor.

Claim 13. (Previously Amended) The multiprocessor computer system according to claim 1 wherein cache coherence mode bits are appended to a processor's storage transactions when transmitted to a connected processor of said multiprocessor computer system.

Claim 14. (Original) The multiprocessor computer system according to claim 13 wherein said cache coherence mode bits are used in a decision determining whether the single originating processor's storage request must be transmitted to additional processors in the system.

Claim 15. (Previously Amended) The multiprocessor computer system according to claim 14 wherein an increase in the effective utilization of the address bandwidth of the buses used to interconnect the processors of a multiprocessor system allows movement of workload among physical processors in a multiprocessor system at the same time as a reduction of the address bandwidth required to maintain cache coherency among all the processors is caused.

Claim 16. (Cancelled)

Claim 17. (New) A method of mananaging cache coherence of a computer system, comprising:

providing a plurality of logical partitions which are defined based upon computing environment requirements,

defining a plurality of coherent cache regions,

mapping logical partitions to said coherent cache regions, and

determining coherency mode bits for each paritions and writing said coherency mode bits to a state of said partitions, and

associating said coherency mode bits with a partition be dispatched by hypervisor dispatch, and

changing coherency boundaries of one or more of said coherent cache regions directly with coherency mode bits for said coherent cache regions, and

wherein a control program for the dispatch of virtual processors for controlling the size and extent of a required coherency domain changes said coherency boundaries directly with said coherency mode bits.

Claim 18. (New) The method according to claim 17 wherein said coherency boundaries for one or more of said logical partions are changed after a need for a change occurs due to system or workload requirements.

Claim 19. (New) The method according to claim 17 wherein a partition has it matching changed when cache coherency regions are to be added by changing coherency mode bits for that partition to includ a larger region.

Claim 20. (New) The method according to claim 17 wherein if a coherency regsion does not include all nodes of an old regions, then said hypervisor dispatch is stopped, and caches of nodes are selectively purged and choerency mode bits for the partition are changed and then normal hypervisor dispatch is resumed.